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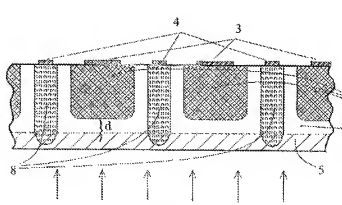
(54) Title: ULTRA THIN BACK-ILLUMINATED PHOTODIODE ARRAY STRUCTURES AND FABRICATION METHODS



(57) Abstract: Ultra thin back-illuminated photodiode array structures and fabrication methods. The photodiode arrays are back illuminated photodiode arrays having a substrate of a first conductivity type having first and second surfaces, the second surface having a layer of the first conductivity type having a greater conductivity than the substrate. The arrays also have a matrix of regions of a first conductivity type of a higher conductivity than the substrate extending from the first surface of the substrate to the layer of the first conductivity type having a greater conductivity than the substrate, a plurality of regions of the second conductivity type interspersed within the matrix of regions of the first conductivity type and not extending to the layer of the first conductivity type on the second surface of the substrate, and a plurality of contacts on the first surface for making electrical contact to the matrix of regions of the first conductivity type and the plurality of regions of the second conductivity type.

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ULTRA THIN BACK-ILLUMINATED PHOTODIODE ARRAY STRUCTURES AND FABRICATION METHODS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor photodiodes, and in particular, to the structures of high performance, back-illuminated photodiode arrays and the methods of fabricating such structures.

2. Prior Art

Conventional photodiode array structures are based on either front illuminated or back illuminated technologies. Figure 1a is a simplified cross section of an exemplary prior art front illuminated photodiode array and Figure 1b is a simplified cross section of an exemplary prior art back illuminated photodiode array. The substrate 1 may be either n-type or p-type material, with opposite conductivity type diffused regions 2 therein. This creates a p-on-n or n-on-p structure, respectively. The anode metal pads 3 for the p-on-n structure (the cathode contacts for the n-on-p structure) are always on the device front surface. The opposite polarity electrode is usually deposited (plated, sputtered, or evaporated) on the chip back side in the case of the front illuminated structure (see metal layer 4, Figure 1a), or is made on the device front surface (see metal pads 4, Figure 1b) using metallized through vias 6,7 in the case of the back illuminated structure. The blanket-type implantation 5 of the back surface of the die of the same conductivity type as the substrate improves both the charge

collection efficiency and DC/AC electrical performance of the devices.

Each of the two approaches - the front illuminated and back illuminated structures - has its own advantages and disadvantages. For example, traditional front illuminated structures like that shown in Figure 1a allow building high performance photodiodes and photodiode arrays, but impose severe constraints on the metal run width. Those constraints limit a design of the front illuminating photodiode array to the use of either a smaller number of elements, or larger gaps between adjacent elements. Note that the metal runs should be accommodated in between adjacent diffusion areas 2 (see Figure 1a).

Back illuminated structures reported recently by several companies take advantage of solder bump technology to electrically connect elements of the array to an external substrate or PC board using the contacts (bumps) on the front surface of the structure. By utilizing solder bump technology, the metal interconnects, which usually reside on top of the active surface between the adjacent elements openings, may be moved to the substrate or PC board upon which the chip is mounted. Such an approach allows minimizing the gaps between adjacent elements of the array, at the same time allowing a virtually unlimited total number of elements. However, several drawbacks of the previously reported back illuminated structures limit their application:

1) First, these structures are usually fabricated using relatively thick wafers (>50 μm) and the resistivity of the material has to be high enough (>1000 Ohm-cm) to deplete the entire volume at zero bias, which is required for many applications;

2) Second, the application of a high resistivity material usually diminishes the photodiode performance with respect to the leakage current and shunt resistance;

3) Third, if a high resistivity material is not used, then the time response will be very long (micro seconds or even longer) because the time response would be determined by the diffusion processes rather than drift processes of the totally depleted structures;

4) Fourth, there are little or no structural features that isolate adjacent cells from each other within the entire thickness of the device, which results in relatively high cross-talk, especially at zero bias.

Summarizing, such parameters as the leakage current, shunt resistance, cross-talk, spectral sensitivity, and temporal response are of main concern for the prior art of back illuminated structures. Additionally, the handling of thin wafers (<50 μm thickness) in the wafer fabrication process is a matter of great concern by itself, and would become increasingly important with the further decrease of the wafer thickness.

BRIEF DESCRIPTION OF THE DRAWINGS

The main ideas of the invention are demonstrated by the accompanying drawings, in which:

Figures 1a and 1b are schematic cross sections of typical, conventional prior art structures for the front illuminated photodiode arrays and back illuminated photodiode arrays, respectively.

Figure 2 is a schematic cross section of an ultra thin, back illuminating photodiode array in accordance with the present invention.

Figure 3 is a schematic cross section of a sample structure of the present invention having a 30μm thick, n-type Silicon wafer.

Figure 4a through 4c illustrate sequential steps of a method for fabricating electrodes of a thin wafer photodiode array structure in accordance with the present invention.

Figure 5 illustrates an exemplary layout of cathode and anode pads across the front surface of the wafer.

Figure 6 is a cross section taken through one of the metal contacts of Figure 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The objectives of the present invention include:

1) To provide a multiple element, back side illuminated 2D-photodiode array with a superior performance of all elements;

2) To provide a fabrication method for the back side-illuminated photodiode array on an ultra thin wafer.

It is therefore an object of this invention to provide a structure for silicon multi-element, 2-D photodiode arrays having greatly improved characteristics over prior art arrays, making it useful in such applications as CT scanner applications, etc.

Another object is to provide a method of fabricating Si devices on ultra thin wafers, which method can be suitable

for fabrication of flip-chip, multi-element, 2-dimensional arrays of silicon photodiodes.

These and other objects of the present invention will become apparent from the following disclosure. In this disclosure, first preferred embodiments of finished diode arrays will be described, and then the preferred method of fabricating the arrays will be described.

Figure 2 is a simplified cross-sectional view of a semiconductor ultra-thin chip photodiode array in accordance with a preferred embodiment of the present invention. The structure is built using either n-type or p-type bulk silicon 1. For brevity, the anode in the case of p-on-n structure or the cathode in the case of n-on-p structure will be referred to as "the first electrode", while the cathode in the case of p-on-n structure and the anode in the case of n-on-p structure will be referred to as "the second electrode."

The material resistivity, thickness of the wafer/die, dopants concentrations and doses, and diffusion conditions are preferably chosen to satisfy the following requirements:

a) The active area (the first electrode) diffusion 2 extends sufficiently close to the back surface of the finished die that the rest of the volume between the diffusion edge and the blanket implant in the die back surface and part of the blanket implant, the space indicated as "d" in the Figure 2, becomes completely depleted at a zero volt bias;

b) The uniform, "blanket" type implantation 5 of the back side of the wafer with the implant of the same polarity as the one of the majority carriers of the wafer bulk 1 provides excellent majority carrier

conductivity across the wafer back side; and ensures a vertical electric field for carrier collection beneath the first electrode to minimize cross talk;

c) The second electrode, diffusion 8, is applied from the front surface of the wafer using the implantation and drive protocols that allow for the diffusion to reach the wafer back side, overlapping thereby with the blanket implantation 5 and providing perfect electrical contacts between the second electrode network across the entire wafer. At the same time, an oxide layer 12 is grown on the front surface, shown in Figure 6, but not shown in the earlier Figures for clarity in the illustrations of the doped regions.

An example of a real structure built using a n-type bulk Si with the resistivity of approximately 400 ohm-cm is shown schematically in Figure 3. At a zero bias, the width of a depletion region is approximately 9μm and extends up to and into (but not through) the blanket implantation 5 in the wafer back side. (See the hatched with dots area 9 in Figure 3. The blanket diffusion 5 is only approximately 0.6μm thick, so the depletion region extends approximately to, but not quite all the way to, the wafer back side.) The built-in potential creates an electric field across the depletion region and facilitates rapid collection of non-equilibrium carriers created by light near the back surface of the die. The non-equilibrium carriers have no or very little possibility of being collected by the electrodes from adjacent cells because:

The electric field near the die back surface, where the carriers photo-generation predominantly occurs is directed perpendicular to the die surface; therefore, the carriers move (drift) primarily toward the junction

of the same cell, having almost no possibility of being trapped by an adjacent cell;

The second electrode diffusion region 8, which is n+ diffusion in the case of Figure 3, spans the entire thickness of the die and acts as an effective carrier isolator from adjacent cells.

The first electrode diffusion 2 may overlap with the second electrode diffusion 8 close to the front surface of the die as shown in Figure 3. This overlapping may significantly decrease the breakdown voltage, which is not important for a zero bias device.

Thus, exemplary representative diffusion profiles of the first electrode 2 and second electrode 8 are shown in Figure 3. The depth of the first electrode diffusion 2 should be less than the finished substrate thickness (typically less than 50 μm, and more typically approximately 30 μm as shown in Figure 3) by an amount that approximately equals the depletion depth for the substrate material 1 at zero bias. The second electrode diffusion 8 should span the entire thickness of the substrate, or at least to a sufficient depth to provide a reliable low resistance contact with the blanket implantation 5 of the back side of the wafer. Note that the dopants 5 and 8 are of the same polarity.

Such a structure may be fabricated starting with a thicker substrate (for example 300 μm) for structural stiffness and integrity during the processing, using three masking steps:

First, as shown in Figure 4a, the second electrode 8 implantation/diffusion is applied followed by a drive. At this stage, the difference in the

final diffusion depths for the first electrodes 2 and second electrodes 8 (approximately 9μm) is formed.

Second, as shown in Figure 4b, the first electrode 2 implantation/diffusion is applied followed by a drive. By the end of this stage, the diffusion profiles 2 and 8 almost reach their final configuration.

Third, as shown in Figure 4c, the second electrode 8 receives an additional enhancement followed by a drive to ensure superior electrical contacts and to activate dopants. At this stage, the profiles of both the cathode and anode diffusions reach their final configurations (see the solid lines and hatched areas in Figure 4c). The diffusion profiles prior to this third step of dopants implantation/diffusion/drive are shown schematically with the dashed lines in Figure 4c. The future back surface of the wafer after back side grinding and polishing is shown schematically with the dashed line 10.

The array is then reduced in thickness by grinding the back side of the array, preferably to provide a substrate thickness of under approximately 50 μm, and more preferably to approximately 30 μm. The final thickness achieved, of course, is preferably selected in accordance with the resistivity of the substrate and the depth of the first electrode diffusion so that the diffusion is spaced away form the back side of the substrate an amount that approximately equals the depletion depth for the substrate material at zero bias. Then a blanket implant of the first conductivity type is made to the back side of the wafer, which implant improves both the charge collection efficiency and DC/AC electrical

performance of the photodiode arrays. Activation of the implant does not significantly alter the first and second electrode diffusions. Alternatively, a diffusion for the back side could be used if desired. The blanket implant is quite thin compared to the depletion region, with the depletion region extending into, but not through, the blanket implant in the final array.

An ideal flatness of the back side surface of the die is very important for many applications, e.g., for CT scanners that require attaching of a scintillator crystal to the back side of the photodiode array. To help satisfy this requirement, the oxide layer 12 is evenly patterned and the metal pads 14 contacting the first electrode 2 and second electrode 8 are evenly spaced across the surface of the die 16 and made the same size to provide identical ball bumping conditions throughout the wafer (see Figures 5 and 6). The oxide layer 12 and metal pads 14 are represented by the larger diameter circles in Figure 5, with the smaller diameter circles describing the contact openings.

The present invention photodiode arrays exhibit very low cross talk because of the excellent isolation of each pixel. Also, because of the small depletion volume, the arrays exhibit low noise and low temperature sensitivity. When used in X-ray systems, they exhibit low radiation damage, and have thermal characteristics similar to scintillators to which they will are mounted. The technique of using a deep diffusion in conjunction with a thin substrate for making electrical contact to the back side of the substrate may, of course be used in other semiconductor devices. While the deep diffusion in the preferred embodiment is of the same conductivity type as the substrate, this is not a limitation

of the invention, as the deep diffusion may be of the opposite conductivity type, if desired.

While preferred exemplary embodiments of the present invention have been disclosed herein, such disclosure is only for purposes of understanding the exemplary embodiments and not by way of limitation of the invention. It will be obvious to those skilled in the art that various changes in fabrication process and structure of the photodiode arrays may be made without departing from the spirit and scope of the invention, as set out in the full scope of the following claims.

CLAIMS

What is claimed is:

1. A back illuminated photodiode array comprising:

a substrate of a first conductivity type having first and second surfaces;

the second surface having a layer of the first conductivity type having a greater conductivity than the substrate;

a matrix of regions of a first conductivity type of a higher conductivity than the substrate extending from the first surface of the substrate to the layer of the first conductivity type having a greater conductivity than the substrate;

a plurality of regions of the second conductivity type interspersed within the matrix of regions of the first conductivity type and not extending to the layer of the first conductivity type on the second surface of the substrate; and,

a plurality of contacts on the first surface for making electrical contact to the matrix of regions of the first conductivity type and the plurality of regions of the second conductivity type.

2. The photodiode array of claim 1 wherein the plurality of regions of the second conductivity type are separated from the second surface of the substrate by an amount that approximately equals the depletion depth for the substrate at zero bias.

3. The photodiode array of claim 1 wherein the plurality of regions of the second conductivity type are

separated from the second surface of the substrate by approximately 9 μm.

4. The photodiode array of claim 2 wherein the substrate is an n-type silicon substrate having a resistivity of approximately 400 ohm-cm.

5. The photodiode array of claim 1 wherein the plurality of contacts are a plurality of ball grid contacts.

6. The photodiode array of claim 5 wherein the plurality of contacts are of substantially equal size evenly distributed across the photodiode array.

7. The photodiode array of claim 1 wherein the matrix of regions of a first conductivity type comprise a rectangular matrix defining an X-Y matrix of square regions, each square region containing a respective one of the plurality of regions of the second conductivity type.

8. The photodiode array of claim 7 wherein doping forming the matrix of regions of a first conductivity type and the plurality of regions of the second conductivity type overlap.

9. The photodiode array of claim 1 wherein the substrate has a thickness of less than approximately 50 μm.

10. The photodiode array of claim 1 wherein the substrate has a thickness of approximately 30 μm.

11. The photodiode array of claim 1 wherein the substrate is a silicon substrate.

12. A back illuminated photodiode array comprising:

a substrate of a first conductivity type having first and second surfaces and a thickness of less than approximately 50 μm;

the second surface having a layer of the first conductivity type having a greater conductivity than the substrate;

a rectangular matrix of regions of a first conductivity type of a higher conductivity than the substrate extending from the first surface of the substrate to the layer of the first conductivity type on the second surface of the substrate, the rectangular matrix defining an X-Y matrix of rectangular regions;

a plurality of regions of the second conductivity type interspersed within the matrix of regions of the first conductivity type, each region of the second conductivity type being within a respective square region defined by the rectangular matrix of regions of a first conductivity type; and,

a plurality of contacts on the first surface for making electrical contact to the matrix of regions of the first conductivity type and the plurality of regions of the second conductivity type.

13. The photodiode array of claim 12 wherein the plurality of regions of the second conductivity type are separated from the second surface of the substrate by an amount that approximately equals the depletion depth for the substrate at zero bias.

14. The photodiode array of claim 13 wherein the plurality of regions of the second conductivity type are separated from the second surface of the substrate by approximately 9 μm.

15. The photodiode array of claim 13 wherein the substrate is an n-type silicon substrate having a resistivity of approximately 400 ohm-cm.

16. The photodiode array of claim 12 wherein the plurality of contacts are a plurality of ball grid contacts.

17. The photodiode array of claim 16 wherein the plurality of contacts are of substantially equal size substantially evenly distributed across the photodiode array.

18. The photodiode array of claim 12 wherein doping forming the matrix of regions of a first conductivity type and the plurality of regions of the second conductivity type overlap.

19. The photodiode array of claim 12 wherein the substrate has a thickness of approximately 30 μm.

20. The photodiode array of claim 12 wherein the substrate is a silicon substrate.

21. A method of fabricating a photodiode array comprising:

providing a semiconductor substrate having first and second surfaces;

providing a first region in the form of a matrix of regions of a first conductivity type of a higher conductivity than the substrate, including a high temperature diffusion, the first region extending into the substrate from the first surface;

providing a plurality of regions of the second conductivity type interspersed within the matrix of regions of the first conductivity type, including an additional high

temperature diffusion, the second region extending into the substrate from the first surface a shorter distance than the first region;

grinding the substrate from the second surface to reduce the thickness of the substrate and to expose the matrix of regions of a first conductivity type and not the plurality of regions of the second conductivity type at the second surface of the substrate;

providing a layer of the first conductivity type having a conductivity greater than the substrate on the second surface of the substrate; and,

providing a plurality of electrical contacts at the first surface for the first region in the form of a matrix of regions of a first conductivity type and the plurality of regions of the second conductivity type.

22. The method of claim 21 wherein the layer of the first conductivity type having a conductivity greater than the substrate on the second surface of the substrate is provided by implantation.

23. The method of claim 21 wherein the substrate is ground to a thickness separates the plurality of regions of the second conductivity type from the second surface of the substrate by an amount that approximately equals the depletion depth for the substrate at zero bias.

24. The photodiode array of claim 21 wherein the plurality of regions of the second conductivity type are separated from the second surface of the substrate by approximately 9 μm.

25. The method of claim 23 wherein the substrate provided is an n-type silicon substrate having a resistivity of approximately 400 ohm-cm.

26. The method of claim 21 wherein the plurality of contacts are a plurality of ball grid contacts.

27. The method of claim 26 wherein the plurality of contacts are of substantially equal size evenly distributed across the photodiode array.

28. The method of claim 21 wherein the substrate is ground to a thickness of less than approximately 50 μm.

29. The method of claim 21 wherein the substrate is ground to a thickness of approximately 30 μm.

30. A method of fabricating a photodiode array comprising:

providing a silicon substrate having first and second surfaces;

providing a first region in the form of a matrix of regions of a first conductivity type of a higher conductivity than the substrate, including a high temperature diffusion, the first region extending into the substrate from the first surface;

providing a plurality of regions of the second conductivity type interspersed within the matrix of regions of the first conductivity type, including an additional high temperature diffusion, the second region extending into the substrate from the first surface a shorter distance than the first region;

providing additional doping of the first region, including a further high temperature diffusion;

grinding the substrate from the second surface to reduce the thickness of the substrate to less than approximately 50 μm and to expose the matrix of regions of a first conductivity type and not the plurality of regions of the second conductivity type at the second surface of the substrate;

providing a layer of the first conductivity type having a conductivity greater than the substrate on the second surface of the substrate; and,

providing a plurality of electrical contacts at the first surface for the first region in the form of a matrix of regions of a first conductivity type and the plurality of regions of the second conductivity type.

31. The method of claim 30 wherein the layer of the first conductivity type having a conductivity greater than the substrate on the second surface of the substrate is provided by implantation.

32. The method of claim 30 wherein the substrate is ground to a thickness that separates the plurality of regions of the second conductivity type from the second surface of the substrate by an amount that approximately equals the depletion depth for the substrate at zero bias.

33. The photodiode array of claim 30 wherein the plurality of regions of the second conductivity type are separated from the second surface of the substrate by approximately 9 μm

34. The method of claim 32 wherein the substrate provided is an n-type silicon substrate having a resistivity of approximately 400 ohm-cm.

35. The method of claim 30 wherein the plurality of contacts are a plurality of ball grid contacts.

36. The method of claim 35 wherein the plurality of contacts are of substantially equal size evenly distributed across the photodiode array.

37. The method of claim 30 wherein the substrate is ground to a thickness of approximately 30 μm.

38. A method of fabricating a semiconductor device comprising:

providing a semiconductor substrate of a first conductivity type;

forming the semiconductor device on a first surface of the semiconductor substrate, including forming deep diffusions extending through the substrate from the first surface to a second surface of the substrate; and,

forming a blanket region of the same conductivity type as the deep diffusions on the second surface of the substrate.

39. The method of claim 38 wherein the substrate is of a first conductivity type and the deep diffusions and the blanket region are of a second conductivity type.

40. The method of claim 38 wherein the deep diffusions extending through the substrate are formed by forming diffusions that are deeper than diffusions of the semiconductor device, and grinding the substrate from the second surface to reduce the thickness of the substrate to expose the deep diffusions from the second surface of the substrate.

41. A method of fabricating a semiconductor device comprising:

providing a semiconductor substrate of a first conductivity type; and,

forming the semiconductor device on a first surface of the semiconductor substrate, including forming deep diffusions extending through the substrate from the first surface to a second surface of the substrate.

42. The method of claim 41 wherein the deep diffusions extending through the substrate are formed by forming diffusions that are deeper than diffusions of the semiconductor device but do not extend through the substrate, and grinding the substrate from the second surface to reduce the thickness of the substrate to expose the deep diffusions from the second surface of the substrate.

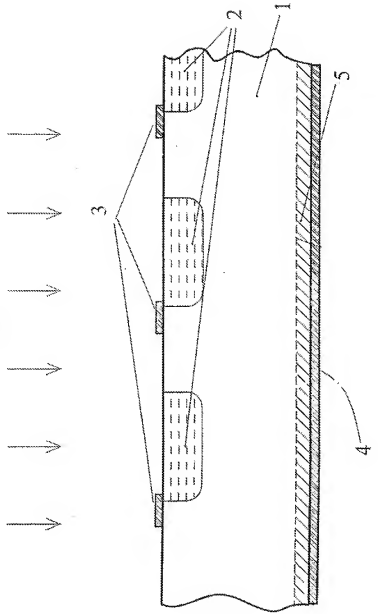

Figure 1a (prior art)

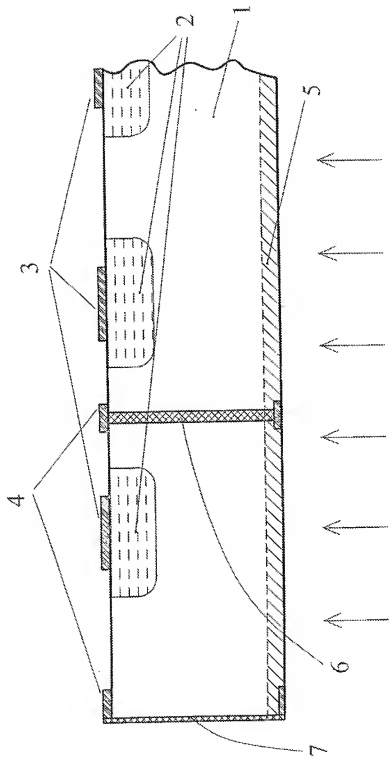

Figure 1b (prior art)

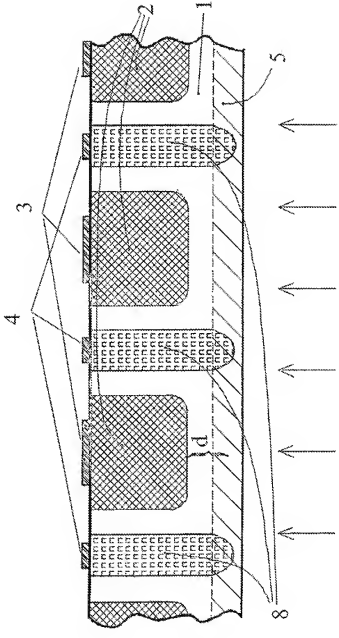

Figure 2

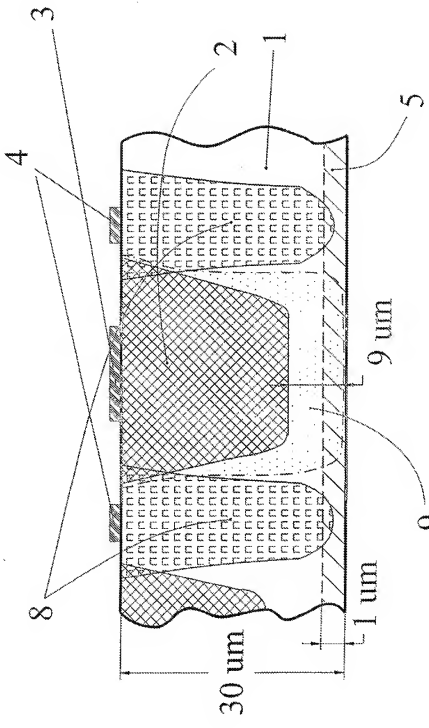

Figure 3

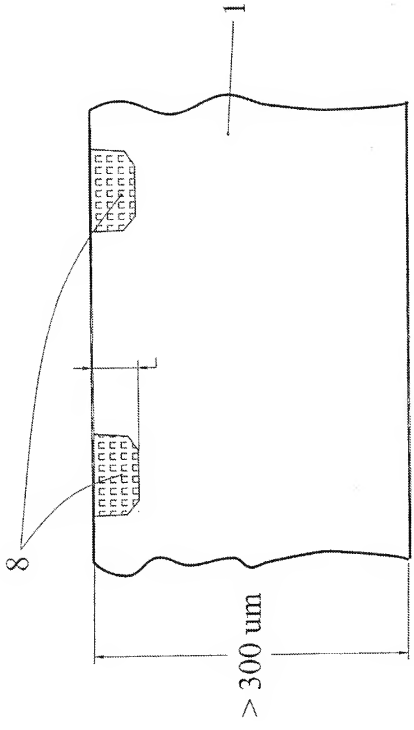

Figure 4a

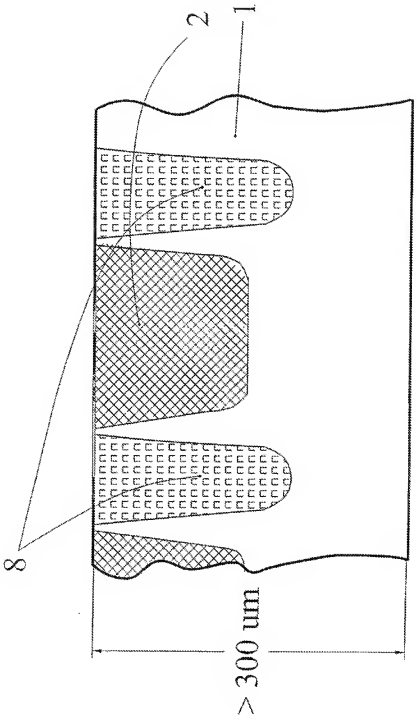

Figure 4b

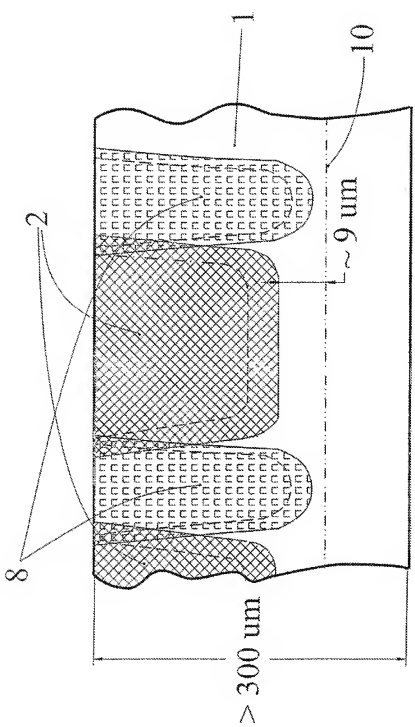

Figure 4c

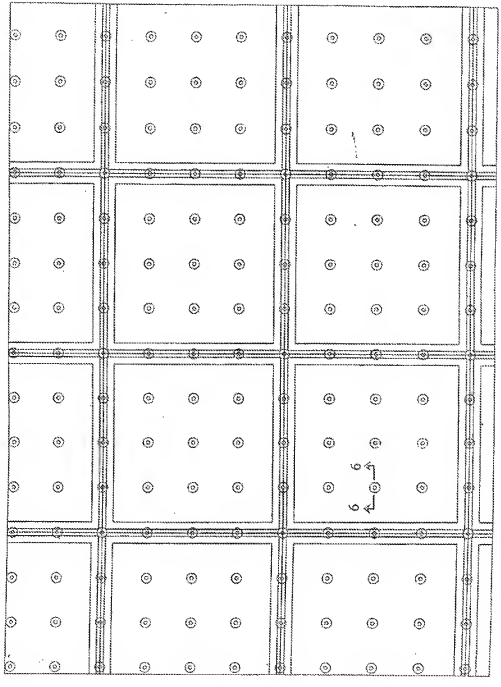

Figure 5

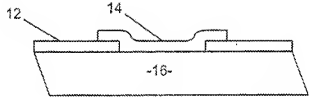

Figure 6

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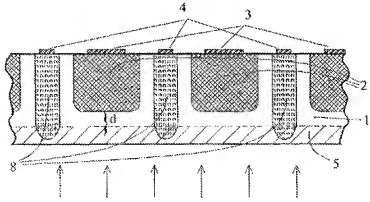
[Continued on next page]

(54) Title: ULTRA THIN BACK-ILLUMINATED PHOTODIODE ARRAY STRUCTURES AND FABRICATION METHODS



(57) Abstract: Ultra thin back-illuminated photodiode array structures and fabrication methods. The photodiode arrays are back illuminated photodiode arrays having a substrate of a first conductivity type having first and second surfaces, the second surface having a layer of the first conductivity type having a greater conductivity than the substrate. The arrays also have a matrix of regions of a first conductivity type of a higher conductivity than the substrate extending from the first surface of the substrate to the layer of the first conductivity type having a greater conductivity than the substrate, a plurality of regions of the second conductivity type interspersed within the matrix of regions of the first conductivity type and not extending to the layer of the first conductivity type on the second surface of the substrate, and a plurality of contacts on the first surface for making electrical contact to the matrix of regions of the first conductivity type and the plurality of regions of the second conductivity type.

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FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR); OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/0352 H01L27/146 H01L31/105

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	YANG M ET AL: "HIGH SPEED SILICON LATERAL TRENCH DETECTOR ON SOI SUBSTRATE" INTERNATIONAL ELECTRON DEVICES MEETING 2001. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC. 2 - 5, 2001, NEW YORK, NY : IEEE, US, 2 December 2001 (2001-12-02), pages 547-550, XP001075585 ISBN: 0-7803-7050-3 page 24.1.1; figures 2,3	41
A	US 5 075 748 A (HISA YOSHIHIRO) 24 December 1991 (1991-12-24) column 2, line 43 - line 55; figure 4 column 4, line 5 - line 18	1-40

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 December 2004	28/12/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Agne, M

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 111 305 A (OTOMO YUSUKE ET AL) 29 August 2000 (2000-08-29) column 6, line 11 - column 7, line 15; figure 3	1-42
A	US 5 538 564 A (KASCHMITTER JAMES L) 23 July 1996 (1996-07-23) column 4, line 23	1-42

INTERNATIONAL SEARCH REPORT

PCT/US2004/020835

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5075748	A	24-12-1991	JP	2237154 A	19-09-1990
			FR	2644293 A1	14-09-1990
			GB	2229036 A ,B	12-09-1990
			US	5156980 A	20-10-1992
US 6111305	A	29-08-2000	JP	11191633 A	13-07-1999
US 5538564	A	23-07-1996	NONE		